IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s):	Luk et al.
Docket No:	YOR920030603US1
Serial No.:	10/751,714
Filing Date:	January 5, 2004
Group:	3663
Examiner:	J. P. Mondt

Title: Amplifiers Using Gated Diodes

REPLY BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
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Sir:

Appellants hereby reply to the Examiner's Answer, mailed July 7, 2009 (referred to hereinafter as "the Examiner's Answer"), in an Appeal of the final rejection of claims 24-28, 36 and 37 in the above-identified patent application.

REAL PARTY IN INTEREST

A statement identifying the real party in interest is contained in Appellants' Appeal Brief.

RELATED APPEALS AND INTERFERENCES

A statement identifying related appeals is contained in Appellants' Appeal Brief.

STATUS OF CLAIMS

A statement identifying the status of the claims is contained in Appellants' Appeal Brief.

STATUS OF AMENDMENTS

A statement identifying the status of the amendments is contained in Appellants' Appeal Brief.

SUMMARY OF CLAIMED SUBJECT MATTER

A Summary of the Invention is contained in Appellants' Appeal Brief.

STATEMENT OF GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A statement identifying the grounds of rejection to be reviewed on appeal is contained in Appellants' Appeal Brief.

CLAIMS APPEALED

A copy of the appealed claims is contained in an Appendix of Appellants' Appeal Brief.

ARGUMENT

Point 10.1

The Examiner asserts that Folmsbee discloses as prior art a charge pump circuit, which is for voltage amplification and which is actually used to increase the amplitude of a voltage communicated to node 125 of the circuit.

Appellants note that Folmsbee teaches that "charge pumps are circuit elements using the pumping action of diode connected MOSFETs and MOS capacitors to *provide a voltage source of higher voltage than the power supplies.*" (Col. 1, lines 29-32; emphasis added.) Thus, as the Examiner apparently acknowledges, *charge pumps provide a voltage source of higher voltage than a power supply.* Folmsbee also teaches "the present invention relates to a low voltage charge pump which operates properly with a low voltage power supply to *provide a high voltage output.*" (Col. 3, lines 58-60; emphasis added.) Folmsbee, however, does *not* disclose or suggest "*amplifying a signal.*" As noted in the Appeal Brief, a *signal line carries information*, as would be apparent to a person of ordinary skill in the art. The IEEE Standard Dictionary of Electrical and Electronic Terms defines a signal as, *for example*, "...carrying

binary true/ false logic values." The line from VDD to node 125 does *not carry information*.

The Examiner also asserts that the arrival of the voltage at node 125 that is subsequently amplified is clearly the first step of the amplification process and hence shows the determination of the user to subject the voltage to the amplification process.

The cited circuit is designed to provide a voltage source, as described above. A step of determining that a signal is to be amplified is *not* disclosed by Folmsbee and is *not* required since 1) *the circuit does not amplify a signal*; and 2) the clock inputs Ø and Ø' are apparently always active and generating the voltage source V_{OUT}. Thus, the step of determining that a voltage on a signal line is to be amplified is *not* required *nor* disclosed by Folmsbee.

The Examiner asserts that, within the context of the amplifier 1300 to which Appellant refers, a small voltage arrives at a node and is consequently amplified, in analogy with the arrival of a voltage VDD-VT at node 125 and its consequent amplification.

As noted above, a *signal line carries information*, as would be apparent to a person of ordinary skill in the art. The IEEE Standard Dictionary of Electrical and Electronic Terms defines a signal as, *for example*, "...carrying binary true/ false logic values." The line from VDD to node 125 does *not carry information*. The voltages VDD and VDD-VT are *not* signals, as defined in the context of the present invention and as is well known in the art.

Point 10.2

The Examiner asserts that the voltage imparted on node 125 is of variable amplitude ("pre-charged to within the supply voltage minus VT") (col. 4, line 31) and hence carries information, both on the exact value or point within the voltage range and on the state of the MOSFET channel 100, such as the resistance of the channel, its impurities, etc., which qualifies it as a signal line according to Appellant's admission.

Contrary to the Examiner's assertion, the voltage imparted on node 125 does *not* "carry information," as defined in the context of the present invention and as is well known in the art. For example, while the voltage on node 125 may be used in an analysis of the overall circuit to determine the resistance of the channel, the voltage on node 125 does *not* carry this information. Moreover, it is unclear how the voltage on node 125 is related to the impurities of the channel nor how the cited voltage *carries information* representing the impurities of the channel. The voltage on node 125 is VDD-VT, a supply voltage (VDD) minus a transistor

threshold voltage (VT), and would not be recognized as a signal by a person of ordinary skill in the art.

Point 10.3

The Examiner asserts that, since the source and drain are short-circuited, they form one terminal. The Examiner asserts, therefore, that the number of terminals equals two and is in no way different from the number of terminals in a gated diode.

Contrary to the Examiner's assertion, the connection of the source terminal to the drain terminal does *not* reduce the terminal count of the device; both terminals still exist, as would be apparent to a person of ordinary skill in the art.

Furthermore, as noted in the Appeal Brief, the Examiner claims that NMOS transistor 110 has an input, an output, and a control terminal. If MOS capacitor 130, which has three terminals, is considered by the Examiner to be a two-terminal device because the source and drain are connected, then NMOS transistor 110 (the alleged isolation device) cannot be considered to comprise three terminals (an input, an output, and a control terminal) since the gate and source are connected. Independent claim 24 requires that *the isolation device have an input, an output and a control terminal.*

Point 10.4

The Examiner asserts that the control signal is strictly separate from the control terminal of the isolation device and that the clock signal Ø' was identified as the "control signal."

The Examiner asserts that the clock signal Ø' was identified as the "control signal" and that the control terminal is the gate of the alleged isolation device 110. Claim 24 also requires, however, that a "control voltage" is applied to the control terminal of the isolation device. The gate of alleged isolation device 110 is connected to the source of alleged isolation device 110; thus, *the control voltage applied to the gate of alleged isolation device 110 is essentially the same signal as the signal to be amplified.* Independent claim 24 requires both a *voltage on a signal line* and *applying a control voltage to the control terminal of the isolation device.* In addition, it is unclear how the configuration of Folmsbee, as interpreted by the Examiner, could function as a *signal amplifier* ***controlled by the control voltage*** *when the control voltage is directly connected to the signal to be amplified.*

Point 10.5

The Examiner asserts that the arrival of a signal at node 125 certainly adds to the gate voltage of the isolation device because there is a direct connection from node 125 to said gate. The Examiner asserts that the supposition by appellant that the voltage at node 125 and at the gate 110 are exactly the same neglects line resistance, inductance and capacitance and hence its applicability depends on signal time scales and particulars of the node-gate connection as well as the properties of the gate itself.

The voltage at the gate of NMOS transistor 110 ***is*** the voltage at node 125, so *no* **addition** of voltages can take place. Thus, even considering the Examiner's reference to the line resistance, inductance and capacitance, signal time scales and particulars of the node-gate connection as well as the properties of the gate itself, the Examiner's assertion appears to be inappropriate.

Claim 25 requires wherein the *control voltage is applied to the control terminal of the isolation device plus an expected voltage for a signal coupled to the input of the isolation device, whereby the isolation device passes signals having voltages less than the expected voltage and does not pass signals having voltages greater than the expected voltage.* Note that the *control voltage is applied to the control terminal* ***and*** *the expected voltage for a signal is coupled to the input.* The Examiner did not clearly address these latter limitations of the cited claim.

Appeal Brief Arguments

Independent Claim 24

Independent claim 24 was rejected under 35 U.S.C. 102(b) as being anticipated by Folmsbee. In particular, the Examiner asserts that Folmsbee discloses determining that a voltage on a signal line (signal line from VDD to node 125) is to be amplified; and modifying voltage on a control line φ' (providing clock input φ' under gate of MOS capacitor 130) (col. 4, lines 1-33), wherein the control line is coupled to a second terminal (source-drain terminal) of a two terminal semiconductor device (MOS capacitor 130),

the two terminal semiconductor device having said second terminal and a first terminal (gate), the first terminal coupled to the signal line, the second terminal coupled to the

control line, wherein the two terminal semiconductor device is adapted to have a capacitance when a voltage on the first terminal is in a first voltage range and to have a lower capacitance when the voltage on the first terminal (gate) is in a second voltage range, wherein said first and second voltage ranges are defined by a threshold voltage, and wherein the control line is adapted to be coupled to a control signal (clock signal φ') and wherein the signal line is adapted to be coupled to a signal and to be an output VOUT of the circuit (through 140); and

wherein an isolation device (NMOS transistor 110) is intermediate the signal line and the two terminal semiconductor device, the isolation device having an input, an output and a control terminal (gate of NMOS transistor 110), the input of the isolation device coupled to the signal line (at node 125) and the output of the isolation device coupled to the first terminal 130 (through node 135), wherein the output of the isolation device is adapted to be the output of "the" circuit, and wherein the method further comprises the step of applying a control voltage to the control terminal of the isolation device, the control voltage being greater than a threshold voltage of the isolation device.

In the Response to Arguments section of the final Office Action, the Examiner asserts that this argument is not persuasive because, even by admission (FIG. 2 and discussion of the present specification), a gated diode is a two-terminal device while having source, gate and drain, with source and drain short-circuited. The Examiner asserts that this terminology is standard in the field of MOS capacitors and MOSFETs.

First, Applicants note that there is NO disclosure in Folmsbee to *determine* that a voltage on a signal line is to be amplified and the Examiner has *not* cited any teaching in Folmsbee that discloses this limitation.

Applicants also note that the Examiner equates the signal line of claim 24 with the line from VDD to node 125. Applicants note that a *signal line carries information*, as would be apparent to a person of ordinary skill in the art. The IEEE Standard Dictionary of Electrical and Electronic Terms defines a signal as, *for example*, "...carrying binary true/ false logic values." The line from VDD to node 125 does *not carry information.*

In the Response to Arguments section of the final Office Action, the Examiner asserts that "no example can possibly be a definition."

Applicants note it was argued that a signal line is defined as a line that "carries information"; this is a definition and *not* an example. Second, the IEEE Standard Dictionary of Electrical and Electronic Terms definition was provided in support of this definition. Finally, contrary to the Examiner's assertion, many terms have more than one definition, as would be apparent to a person of ordinary skill in the art. Applicants used the phrase "for example" to acknowledge that different sources often provide slightly different definitions of a term.

In the Response to Arguments section of the final Office Action, the Examiner asserts that "the variable voltage VDD not only can be used, and actually is used, in the method employing the device by Folmsbee, to convey information on control, because the voltage source VDD is a modified signal carrying information upon arrival at node 125."

Applicants note that Folmsbee teaches that VDD is "a supply voltage." (Col. 4, line 16.) Contrary to the Examiner's assertion, a "supply voltage" is *not a signal*, in accordance with the well known definition of the term and, furthermore, Folmsbee does *not* disclose or suggest that VDD is a signal or that VDD conveys information.

In addition, MOS capacitor 130 is a three terminal device (gate, source, and drain), as would be apparent to a person of ordinary skill in the art. The connection of the source terminal to the drain terminal does *not* reduce the terminal count of the device.

Furthermore, the Examiner claims that NMOS transistor 110 has an input, an output, and a control terminal. If MOS capacitor 130, which has three terminals, is considered by the Examiner to be a two-terminal device because the source and drain are connected, then NMOS transistor 110 cannot be considered to comprise three terminals (an input, an output, and a control terminal) since the gate and source are connected. Independent claim 24 requires that the isolation device have an input, an output and a control terminal.

More importantly, the Examiner equates the signal of independent claim 24 with the signal line from VDD to node 125 in Folmsbee, and that node 125 is considered the input to the alleged isolation device 110. The Examiner, however, also equates the gate of alleged isolation device 110 with the control terminal cited in claim 24. The gate of alleged isolation device 110 is connected to the source of alleged isolation device 110; thus, *the control signal is essentially the same signal as the signal to be amplified.* Independent claim 24 requires both a *voltage on a signal line* and a *control voltage (signal).* In addition, it is unclear how the

configuration of Folmsbee, as interpreted by the Examiner, could function as an amplifier when the control signal is directly connected to the signal to be amplified.

Thus, Folmsbee does not disclose or suggest determining that a voltage on a signal line is to be amplified and does not disclose or suggest wherein the control line is coupled to a second terminal of a two terminal semiconductor device, as required by independent claim 24.

Claim 25

Claim 25 was rejected under 35 U.S.C. 102(b) as being anticipated by Folmsbee. In particular, the Examiner asserts that the limitation is met because "the 'expected' voltage for a signal coupled to the input of the isolation device is the voltage at node 125, which is added to the voltage on the gate of NMOS transistor 110, i.e., the isolation device (col. 4, lines 34-40) the gate thereof being in series with said node 125, and the clock input Φ in a high state adding to the pre-charge voltage at 125 the clock swing of clock input Φ."

The Examiner asserts that "the 'expected' voltage for a signal coupled to the input of the isolation device is the voltage at node 125." The Examiner asserts that this voltage (the voltage at node 125) is then "added to the voltage on the gate of NMOS transistor 110." The voltage at the gate of NMOS transistor 110 ***is*** the voltage at node 125, so *no* addition of voltages can take place. Thus, the Examiner's assertion appears to be inappropriate. In addition, contrary to the Examiner's assertion, the gate (of NMOS transistor 110) is directly connected to node 125 and, therefore, contrary to the Examiner's assertion, the gate is *not* in series with said node 125. Claim 25 requires wherein the *control voltage is applied to the control terminal of the isolation device plus an expected voltage for a signal coupled to the input of the isolation device, whereby the isolation device passes signals having voltages less than the expected voltage and does not pass signals having voltages greater than the expected voltage.*

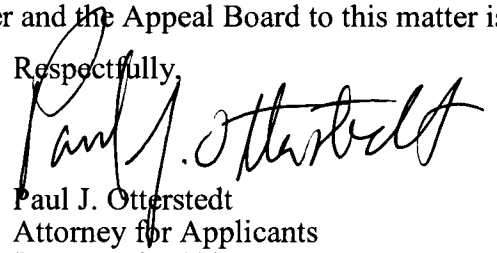
Thus, Folmsbee does not disclose or suggest wherein the control voltage is applied to the control terminal of the isolation device plus an expected voltage for a signal coupled to the input of the isolation device, whereby the isolation device passes signals having voltages less than the expected voltage and does not pass signals having voltages greater than the expected voltage, as required by claim 25.

Conclusion

The rejections of the cited claims under section 102 in view of Folmsbee are therefore believed to be improper and should be withdrawn. The remaining rejected dependent claims are believed allowable for at least the reasons identified above with respect to the independent claims.

The attention of the Examiner and the Appeal Board to this matter is appreciated.

Respectfully,



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CLAIMS APPENDIX

1.-23. (Canceled)

24. A method for amplifying signals, the method comprising the steps of:

determining that a voltage on a signal line is to be amplified; and

modifying voltage on a control line, wherein the control line is coupled to a second terminal of a two terminal semiconductor device, the two terminal semiconductor device having the second terminal and a first terminal, the first terminal coupled to the signal line, the second terminal coupled to the control line, wherein the two terminal semiconductor device is adapted to have a capacitance when a voltage on the first terminal is in a first voltage range and to have a lower capacitance when the voltage on the first terminal is in a second voltage range, wherein said first and second voltage ranges are defined by a threshold voltage, and wherein the control line is adapted to be coupled to a control signal and wherein the signal line is adapted to be coupled to a signal and to be an output; and

wherein an isolation device is intermediate the signal line and the two terminal semiconductor device, the isolation device having an input, an output and a control terminal, the input of the isolation device coupled to the signal line and the output of the isolation device coupled to the first terminal, wherein the output of the isolation device is adapted to be the output, and wherein the method further comprises the step of applying a control voltage to the control terminal of the isolation device, the control voltage being greater than a threshold voltage of the isolation device.

25. The method of claim 24, wherein the control voltage is applied to the control terminal of the isolation device plus an expected voltage for a signal coupled to the input of the isolation device, whereby the isolation device passes signals having voltages less than the expected voltage and does not pass signals having voltages greater than the expected voltage.

26. The method of claim 24, wherein the isolation device comprises a Field Effect Transistor (FET) and wherein the FET is adapted to be turned on when voltage on the signal line is below a predetermined value, and is adapted to be turned off when voltage on the first terminal

of the two terminal semiconductor device is above a predetermined value.

27. The method of claim 26, wherein the FET is an n-type FET, wherein the control terminal of the FET is the gate of the FET, and wherein the step of applying a control voltage to the control terminal of the isolation device further comprises the step of applying a voltage above a threshold voltage to the gate of the FET.

28. The method of claim 26, wherein the FET is a p-type FET, wherein the control terminal of the FET is a gate, and wherein the step of applying a control voltage to the control terminal of the isolation device further comprises the step of applying a voltage below a threshold voltage to gate of the FET.

29.-35. (Canceled)

36. The method of claim 24, further comprising the step of generating the control voltage by using at least a reference voltage and the control voltage.

37. The method of claim 36, wherein the step of generating the control voltage further comprises the step of generating the reference voltage by using one or more of the following: a ground voltage; a power supply voltage; the signal; the threshold voltage; one or more additional threshold voltages; one or more temperature signals; and the control voltage.

38.-42. (Canceled).

EVIDENCE APPENDIX

There is no evidence submitted pursuant to § 1.130, 1.131, or 1.132 or entered by the Examiner and relied upon by appellant.

RELATED PROCEEDINGS APPENDIX

There are no known decisions rendered by a court or the Board in any proceeding identified pursuant to paragraph (c)(1)(ii) of 37 CFR 41.37.